A 12-15 GHz HIGH GAIN AMPLIFIER DESIGN USING SUBMICRON GATE GaAs FIELD EFFECT TRANSISTORS*

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Abstract

An amplifier covering 12-15 GHz with 22 dB gain and less than 5.0 dB noise figure using GaAs FETs with submicron gate length was constructed. Techniques used for device characterization and amplifier circuit synthesis along with measured data are presented.

Introduction

Gallium Arsenide Shottky-barrier gate field effect transistors (GaAs FETS) offer several potential advantages for microwave amplifier design.[1] Particularly important characteristics include relatively low noise figure, improved output power associated with low noise figure, and input to output isolation inherent in these three terminal devices. A relatively new device, the GaAs FET with submicron gate length (nominally 0.5 micron), offers improved gain and noise figure relative to more conventional one micron devices for applications above 10 GHz. A 12 to 15 GHz amplifier is described which was constructed using 0.5 micron devices from Nippon Electric Company (the NEC 388 GaAs FET). The amplifier design consists of four nearly identical single-ended stages cascaded to achieve 22 dB gain over the 12-15 GHz band. Noise figure ranged from 3.8 to 5.0 dB, and power output was +5 to +6 dBm at 1 dB gain compression. The amplifier was constructed using unpackaged GaAs FET chips with thin film microstrip input and output circuit realizations on fused silica substrates. The measurement and characterization of the devices in this configuration is described, and techniques employed for circuit synthesis are presented. Techniques employed are applicable to 12-18 GHz amplifier design, and 12-18 GHz amplifier results are also presented.

Amplifier Design Approach

This amplifier development effort included device electrical characterization, amplifier design, and amplifier fabrication and evaluation. Precise electrical characterization of the new devices was a prequesite to circuit synthesis. After such characterization, design procedures similar to those reported by Liechti[2], Ku and Podell[3], and Walker[4] for frequencies of 12 GHz and below were expected to be applicable to this 12-15 GHz design.

Techniques for device characterization have been described by Gelnovatch[5], although it is appropriate to report certain peculiar problems encountered in these measurements which were conducted over 12-18 GHz. The GaAs FET was mounted on a metal rib of 0.5 mm width which constitutes RF ground; the source contact was RF grounded and the gate and drain terminals were connected directly to 50 ohm input and output transmission lines. It was found to be beneficial to incorporate dc bias chokes (RF short circuited lines of $\lambda/4$ length at 18 GHz) and blocking capacitors integral to the microstrip, as shown in Figure 1. These bias circuits were designed to minimize the loading of the test fixture and to reduce the number of coaxial transitions and the electrical line lengths inherent in the total test fixturing. Of particular significance is that this approach simplifies establishment of an accurate reference plane for device scattering parameter determination.

Measured parameters of the NEC V388 device are presented in Table 1. It should be cautioned that this data is based on a small sampling of devices, and that it is dependent on the precise device mounting technique and the parasitics introduced by bonding wires inherent in the fixture.

The basic circuit design approach was to synthesize relatively simple two-pole input and output matching circuits. These circuits were optimized to provide constant gain as a function of frequency using an internally developed computer-aided optimization program (THRIFTY). Additionally, the input circuit was designed to provide a best estimate of optimum noise match, although direct measurement of optimum noise match source impedances has not yet been accomplished at 15 GHz.

The resultant circuit is given in Figure 2. It consists of a high impedance line of appropriate electrical length formed with a 0.02 mm diameter gold bonding wire and a pair of short circuited shunt stubs in parallel, etched directly onto the microstrip circuit. The 22 dB gain amplifier was achieved using four essentially identical stages in series, with isolators at the input and output to reduce terminal VSWRs, as shown in Figure 3.

The high gain amplifier exhibited 19 dB minimum gain upon initial turn-on. Relatively large (5 dB) ripple was attributed to interstage matching discontinuities between individual stage substrates. These substrates are of 0.4 mm thickness, with a typical mechanical gap between stages being 0.1 mm and interconnection accomplished with a 0.5 mm wide gold ribbon. The amplifier gain ripple was reduced to 3 dB (± 1.5 dB) by compensating the interstage discontinuities with small additional capacitance at the discontinuities. This was the only "alignment" necessary on this first prototype amplifier.

Electrical results are presented in Figure 4. The noise figure of 3.8 to 5.0 dB is considered to be of particular significance. This is, to our knowledge, superior to competitive technology for 12-15 GHz bandwidth. It is also important to note that the output power and third order intermodulation intercept point associated with this low noise figure are substantially (> 10 dB) above that of low noise travelling wave tubes or tunnel diode amplifiers. It should be added that the measured noise figure increase of 3.8 to 5.0 dB as frequency increased from 12 to 15 GHz is thought to

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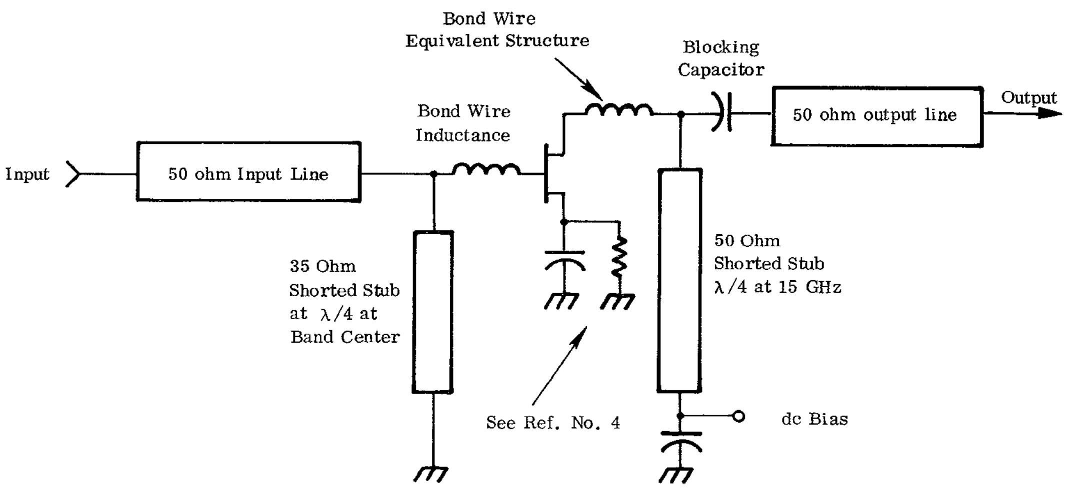

Figure 2

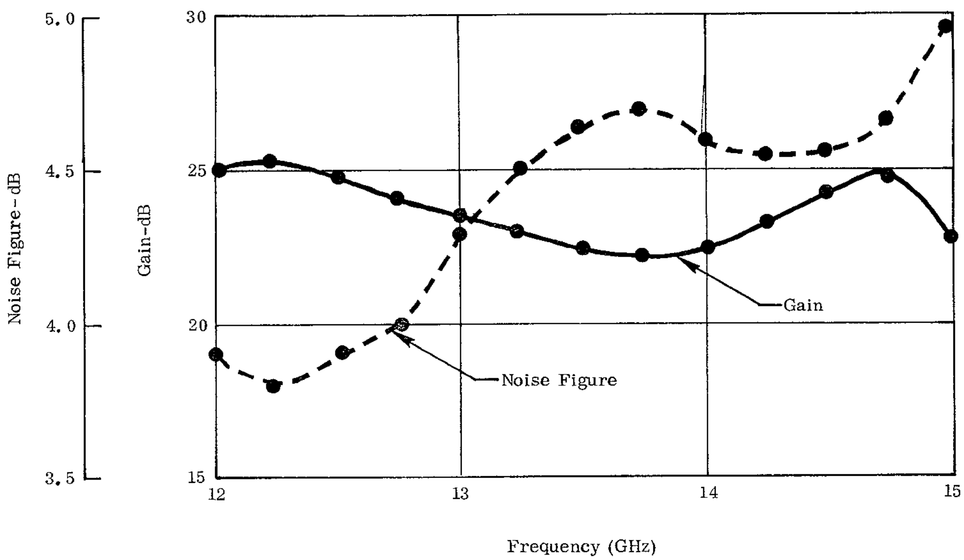

Figure 4

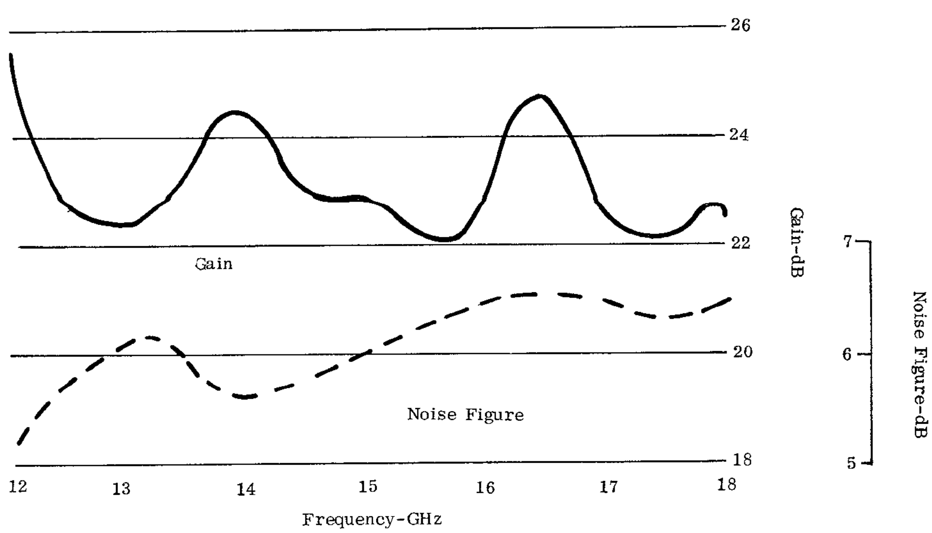

Figure 5

exceed the noise figure increase inherent in the GaAs FET device itself, and that further circuit optimization is possible near 15 GHz.

Using similar techniques, a gain module was designed to operate over 12-18 GHz. Performance of 4 cascaded gain modules, including isolators is given inFigure 5. This is the first reported high gain transistor amplifier covering Ku-Band.

Conclusion

A multistage 12-15 GHz amplifier design using 0.5 micron GaAs FETs has been presented. A noise figure of 5.0 dB max over 12-15 GHz was achieved. Design techniques applicable to the general FET amplifier design problem in the 12-18 GHz range have also been reported.

Acknowledgement

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TABLE 1

NEC V388 1/2 MICRON GaAs FET
MEASURED DATA 12-18 GHz

Freq GHz	S_{11} MAG	ANG	S_{21} MAG	ANG	S_{12} MAG	ANG	S_{22} MAG	ANG	G_{max} dB
12.0	0.60	-140	1.99	-10	0.07	-13	0.57	-37	9.62
13.0	0.63	-147	1.77	-26	0.06	-24	0.60	-55	9.08
14.0	0.66	-155	1.60	-45	0.06	-33	0.63	-69	8.74
15.0	0.67	-149	1.41	-58	0.07	-39	0.71	-72	8.59
16.0	0.57	-157	1.35	-72	0.07	-43	0.73	-66	7.63
17.0	0.56	176	1.41	-88	0.08	-54	0.69	-70	7.43
18.0	0.62	165	1.24	-106	0.09	-66	0.64	-92	6.23

Bias: V_{ds} = 3.5 volts, I_D = 25 mA, gm ≈ 22 mmho

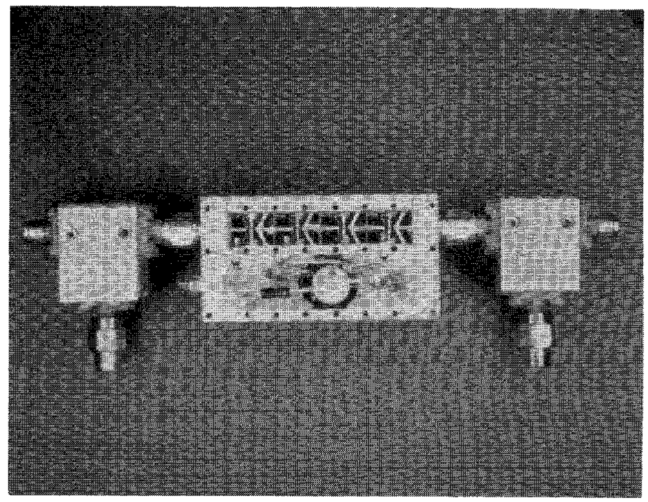

Figure 3

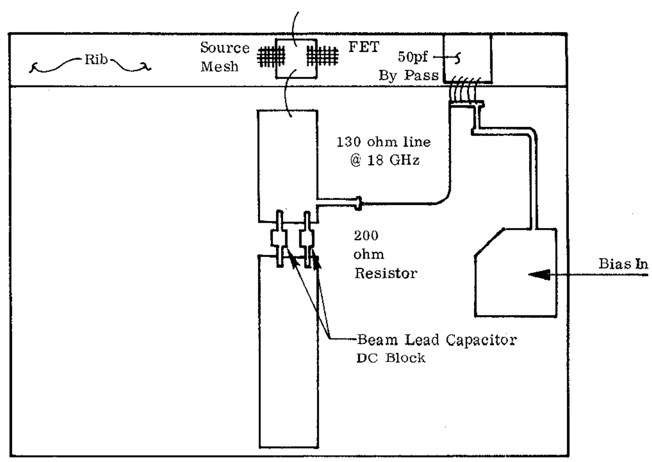

Figure 1

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